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DESIGN OF CARRY PREDICTION-BASED ADDER USING FIXED WIDTH TECHNIQUE

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Abstract:

Parallel Distributed Arithmetic forms are core of many important Digital Signal Processing (DSP) functions such as linear and circular convolutions, correlation, digital filtering, and discrete trigonometric transforms. In this project, a novel PDA-based structures is proposed based on efficient truncation model. A hardware-efficient fixed-width PDA-based inner-product structures was obtained by using approximate Look-Up Tables (LUTs), Adder Trees (ATs), and Wallace-like Shift-AT (SAT) with truncated operands. In this project, three different inner product architectures is implemented based on their variants like area, delay etc. The effectiveness of the proposed method is designed using XilinxISE14.7 software.

Keywords: Approximate computation, Distributed Arithmetic (DA), Look up Table, Adders.

INTRODUCTION

Mobile devices and DSP hardware requires low power, area, efficient designs for better performances. Fixed-point VLSI systems have Digital Signal processing (DSP) algorithms to be implemented. These designs require adder tree (AT) which are commonly used in parallel designs. The shape of adder tree is different from SAT. Consequently, word- length grows in a different order in SAT and AT. Multiplier

deals with partial products. Hence, we prefer adder trees to get complex design easy. But the fixed width adder tree and multiplier are not appropriate when we compared regarding schemes. Since, the fixed width AT produces different shaped matrices compared to the fixed width multiplier. However, direct truncation and post truncation methods are employed to the FX-AT and FL-AT conventionally. In direct truncation (DT), one lower order bit of each adder output of full width adder tree is post truncated and in case of post truncation final adder output of FL-AT lower adder bits are truncated. However, these adder trees are implemented using Ripple Carry Adder to get accurate results. It is necessary to have a different approach for developing efficient FX-AT design which is currently missing in the literature. An efficient FX-AT design certainly help to improve the efficiency of dedicated VLSI systems implementing complex DSP algorithm.

LITERATURE SURVEY

IMPrecise adders for low-power Approximate CompuTing by Vaibhav Gupta, DebabrataMohapatra, Sang Phill Park, Anand Raghunathan and KaushikRoy:Low-power is an imperative requirement for portable multimedia devices employing various signal processing algorithms and architectures. In most multimedia applications, the final output is interpreted by human senses, which are not perfect Energy-efficient signal processing via algorithmic noise-tolerance, by R. Hegde ; N.R. Shanbhag: In this a framework for lowenergy digital signal processing (DSP) where the supply voltage is scaled beyond the critical voltage required to match the critical path delay to the throughput Design of low-power high-speed truncation-error tolerant adder and its application in digital signal processing, by N. Zhu, W. L. Goh, W. Zhang, K. S. Yeo, and Z. H. Kong: In modern VLSI technology, the occurrence of all kinds of errors has become inevitable. By adopting an emerging concept in VLSI design and test, error tolerance (ET), a novel error-tolerant adder (ETA) is proposed Inexact designs for approximate low power addition by cell replacement, by H. A. F. Almurib, T. N. Kumar, and F. Lombard:,It has three designs of an inexact adder cell for approximate computing. These cells require a substantially smaller number of transistors compared to an exact full adder cell as well as known inexact designs Accuracy configurable adder for approximate arithmetic designs by A. B. Kahng and S. Kang Approximation can increase

performance or reduce power consumption with a simplified or inaccurate circuit in application contexts where strict requirements are relaxed. A low-power, high-performance approximate multiplier with configurable partial error recovery by Cong Liu ; Jie Han ; FabrizioLombard;Approximate circuits have been considered for error-tolerant applications that can tolerate some loss of accuracy with improved performance and energy efficiency. Multipliers are key arithmetic circuits in many such applications such as digital signal processing (DSP). In this a novel approximate multiplier with a lower power consumption and a shorter critical path than traditional multipliers is proposed for high-performance DSP applications

EXISTING SYSTEM

The existing fixed-width DA-based structure processes almost the same amount of bits as the full width structure and offers a marginal area-delay saving but introduces relatively a larger amount of error in the inner-product output. Using logic approximation along with post-truncation in the fixed-width AT and WSAT, the area-delay complexity of fixed-width structure could be reduced marginally over the post-truncation fixed-width structure but at the cost of higher accuracy loss compared to other methods. Therefore, the existing truncation models and logic approximation do not lead to an efficient fixed-width structure.

Disadvantages:

- Area increases
- High accuracy loss

PROPOSED SYSTEM

The proposed structure-1 consists of ALUTs, AT-2, and post-truncated WSAT. Each LUT unit Comprises (N/4) LUTs of 16-words each. Outputs of (N/4) LUTs of each LUT unit are sent to an AT-2 to compute one partial inner product. The approximate-WSAT of proposed structure-1 uses post-truncation of AT outputs. Instead of post truncation, the required AT output word size also attained by the truncation of AT input operand. Bit width of the set of LUTs associated with the AT is reduced similar to LUT approximation of proposed structure-1 such that the AT outputs are directly sent to the approximate-WSAT without post-truncation. Based on this approach, a fixed width DA structure (proposed structure-II) which is shown in below figure.

The proposed structure-1 and structure-2 employ pre truncation and post-truncation at

the AT and SAT stages. To achieve the higher bit saving, we have performed pre operand truncation in proposed structure-3. The structure is modified by replacing the AT by AT-1 to obtain the proposed structure-3. AT-1 uses input operands truncated by *p* bits which is one bit higher than input-operand truncation bits of AT-2. Bit width of ALUTs associated with AT-1 is further reduced by *p* bits. The proposed structures along and the other approximate structure based on ALUT offer higher bit saving than the structures based on FLUT, but the ALUT introduces a substantial amount of error into the AT output primarily due to missing carries originating from the truncated part of the LUT word.

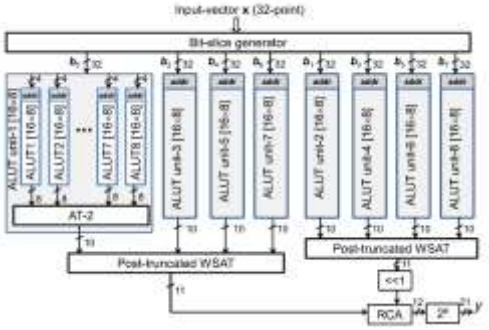


Fig: Block diagram of proposed structure-1

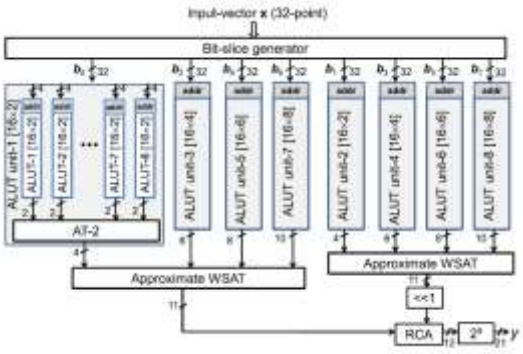


Fig: Block diagram of proposed structure-2

Advantages:

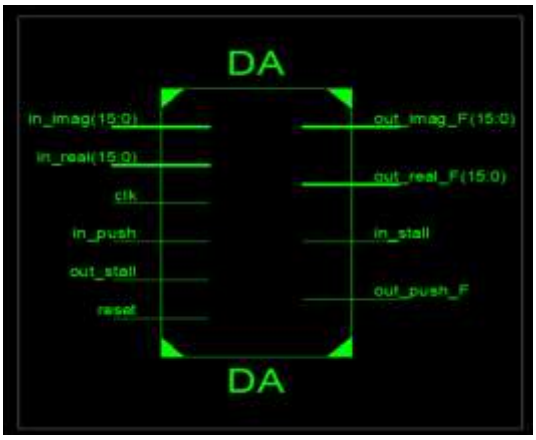
- By using the proposed design, area will be less.
- Error rate is less.
- Higher bit saving can be obtained in proposed structure2.

Applications:

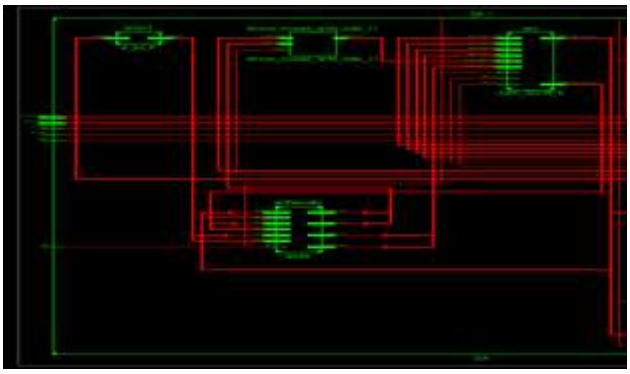
- DSP applications
- Image filtering

SIMULATION RESULTS

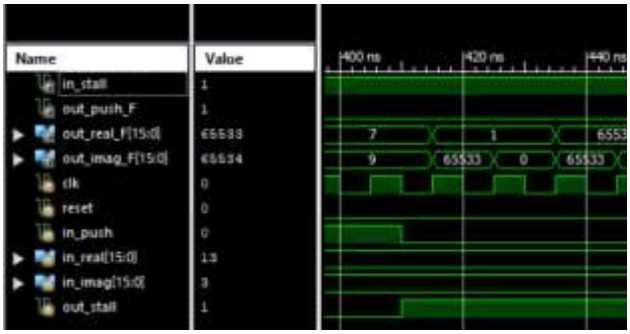
RTL



INTERNAL BLOCK DIAGRAM



SIMULATION RESULTS



CONCLUSION

We have proposed three variants of approximate PDA-based structures based on an efficient truncation model. To achieve higher bit saving with relatively less truncation error, we have presented here a novel approach using approximate LUTs, ATs, and WSAT with truncated operands to obtain hardware-efficient fixed-width PDA-based inner-product structures. We find that the proposed structure using ALUT and approximate AT offers nearly 20% higher bit saving, 20% saving in ADP and offers relatively less truncation error than the existing structures. The proposed structure-2 using ALUT, ATs, and proposed SAT offers nearly 50% higher bit saving, 61% ADP saving and offers nearly the same accuracy compared to the existing DA-based structures [10]. Proposed structure-3 offers nearly 60% higher bit saving and calculates the outputs with almost the same or marginally less accuracy than the existing structure for higher coefficient word lengths. The FIR filters based on the proposed structure-1 and proposed structure-2, respectively, offer nearly 27% and 42% less ADP than the similar existing structures and calculate output with higher or nearly the same accuracy.

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